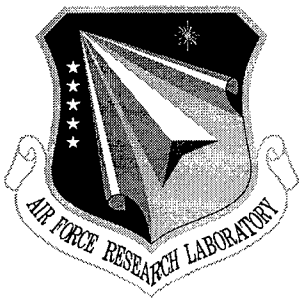
AFRL-SN-RS-TR-1998-68
In-House Report
May 1998



OPTICALLY GUIDING SUBSTRATES FOR LOW COST OPTICAL INTERCONNECTS IN STACKED MULTICHIP MODULE AND CHIP SCALE PACKAGING

Franz Haas and Paul Cook

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REPORT DOCUMENTATION PAGE			Form Approved OMB No. 0704-0188

1. AGENCY USE ONLY *(Leave blank)*	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	May 1998	In House Oct 93 - Sep 96

4. TITLE AND SUBTITLE
OPTICALLY GUIDING SUBSTRATES FOR LOW COST OPTICAL INTERCONNECTS IN STACKED MULTICHIP MODULE AND CHIP SCALE PACKAGING

5. FUNDING NUMBERS
C - In-House
PE - 62702F
PR - 4600
TA - P3
WU - 30

6. AUTHOR(S)
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7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
Air Force Research Laboratory/SNDP
25 Electronic Parkway
Rome NY 13441-4515

8. PERFORMING ORGANIZATION REPORT NUMBER
AFRL-SN-RS-TR-1998-68

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)
Air Force Research Laboratory/SNDP
25 Electronic Parkway
Rome NY 13441-4515

10. SPONSORING/MONITORING AGENCY REPORT NUMBER
AFRL-SN-RS-TR-1998-68

11. SUPPLEMENTARY NOTES
Air Force Research Laboratory Project Engineer: Franz Haas/SNDP/(315) 330-2131

12a. DISTRIBUTION AVAILABILITY STATEMENT
Approved for public release; distribution unlimited.

12b. DISTRIBUTION CODE

13. ABSTRACT *(Maximum 200 words)*

A novel method of integrating an optically guiding material into the support structure of the computer creates a high performance data buss while reducing the complexity and cost of implementing an optical interconnect scheme. This report discusses the use of optically guiding materials in both multichip module and chip-scale packaging schemes. In both implementations, closely spaced optical data channels are guided from one plane of electronic circuits to another without the need of costly micro-optics and complex alignment requirements.

14. SUBJECT TERMS
Optical Interconnects, Multichip Modules, Computer Design

15. NUMBER OF PAGES
44

16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
UNCLASSIFIED	UNCLASSIFIED	UNCLASSIFIED	UL

Standard Form 298 (Rev. 2-89) (EG)
Prescribed by ANSI Std. 239.18
Designed using Perform Pro, WHS/DIOR, Oct 94

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Abstract

Many military computational tasks require a large amount of processing capability while operating in unique environments such as in aircraft, missiles, satellites, and unmanned air vehicles (UAV's). The complex missions and extreme environments push the capabilities of standard computer design specifically in the areas of extremely small size, high processing power, high reliability, low heat dissipation and low cost. Real-time image processing, radar signal processing, and threat analysis are a few of the mission tasks continually requiring more computing power in smaller computer systems.

This report describes an approach to reduce computer size while increasing operating speed by integrating high speed optical data busses with high speed electronic processors. Wires used to send information between computer boards are replaced by optical interconnects which operate at greater speeds, at lower power and with a much smaller footprint than traditional electronic solutions.

A novel method of integrating an optically guiding material into the support structure of the computer creates a high performance data buss while reducing the complexity and cost of implementing an optical interconnect scheme. This report discusses the use of optically guiding materials in both multichip module and a chip-scale packaging schemes. In both implementations closely spaced optical data channels are guided from one plane of electronic circuits to another without the need of costly micro-optics and complex alignment requirements.

1. Introduction

The application of electro-optics to Air Force computer requirements were analyzed in RL-TR-97-193[1]. This report explored future Air Force airborne computing requirements, the advantages of enhancing electronic systems with optical technologies, and the appropriate insertion point for those optical technologies. Space-time adaptive processing (STAP) was identified as a computationally intensive problem where the desired performance could not be achieved with electronic computational methods alone. Optical enhancements in the form of specific function modules and the use of optical interconnects were proposed solutions to meet the STAP requirements. It is evident that the hybrid elecro-optical computing technology can be applied to a range of applications to increase computational speed, to reduce computer size, and possibly to increase system reliability and to reduce power consumption.

1.1 Optical Interconnects

1.1.a Background

The use of light as a medium for transmitting information between processing circuitry inside of a computer system has been the goal of many research efforts[2,3,4,5]. By using light instead of traditional electronic signals propagating down wires, the number, density, and speed of data transmitted can be greatly increased leading to advances in the operating speed and processing power of computer systems. However, the implementation of optical interconnects in computer systems have been stalled by the lack of an adequate means of controlling the propagation of the light between circuitry and by the lack of an efficient means of aligning this hybrid electro-optical computer system.

The limits of electronic interconnects are well documented[6,7]. Wires take up too much space, they can not be placed close to one another without cross coupling of the electronic signals, and they have a characteristic capacitance which limits the rate at which data can be sent. As integrated circuits become faster and as computers become smaller, the electronic interconnects become the performance limiting factor of the system.

1.1.b Technical Issues

Any optical interconnect scheme must meet certain design requirements. The scheme must provide for the propagation of the optical signals from one location to another in a controlled manner. It must provide for a means for insuring that the light in one data path does not end up in another data path at the receiving circuitry resulting in a confusion of the transmitted signals. Enough light must be received at the receiving circuitry to discern the data transmitted. The method of initially aligning the computer system must be within the capabilities of the computer manufacturers. And finally, the alignment of the computer must be maintained through reasonable vibration and heating cycles.

Typically, an optical interconnect scheme would consist of optical emitters, photodetectors and a lens system which could be a refractive lens, a diffractive optic element or a holographic element. An optical interconnect is comprised of either a single high speed emitter and detector system or arrays containing of many slower emitters and detectors operating in parallel. The lens would collect the light emitted from one optical source and focus it onto a corresponding photodetector. In some designs more than one optical lens device is used to control the collection and redirection of the optical signals. The resulting optical interconnect scheme is typically expensive to manufacture and extremely hard to align and is susceptible to misalignment due to jarring or thermal expansion of any of the elements. Optical interconnects have not developed into a commercializable technology due to the cost and complexity of the schemes proposed.

There exists a need for a method of transmitting optical signals inside of a computer system in a controlled manner that is easily aligned. This report explores the use of optically guiding material in stacked MCM and stacked chip architectures to provide a high performance data buss which is easily aligned and relatively inexpensive.

1.1.c Implementation

1.1.c.i Multichip Module Interconnects

MCM's are a method of achieving a high level of computing power in a small package[8]. Improvements in circuit densities, small system volumes, integration of different circuit technologies, and high system data rates have been the driving forces behind MCM development. Applications range from portable computer and communications devices to missile, aeronautical, and satellite based processors. Increasingly, these applications are moving towards a stacked MCM architecture to provide a large amount of processing power in a small volume[9,10].

One of the critical information bottlenecks in such a stacked MCM computer system is the MCM-to-MCM interconnect. Traditional methods of running electronic data lines between modules will not be able to meet the data throughput requirements of these high speed computing platforms. While many MCM substrates have electrical properties supporting high speed electronic signals on a single module, the transmission of signals between modules is limited in overall number, density, and data rate. The electronic interconnects originating from chips on the MCM must be brought to the MCM's edge and MCM-to-MCM connections are established along perimeter of the MCM. The sum of the distance from the center of one MCM to the edge, the MCM-to-MCM distance, and the distance from the edge to the receiving chip represents a significant time delay for an electronic signal at the current data rates. The limited perimeter size also represents a limit to the number of interconnects that can be established.

An optical interconnect scheme for stacked MCM computer platforms is outlined in Chapter 4 of this report. It addresses a method of guiding optical signals between modules with a very high data throughput, high optical throughput, with a straightforward method of aligning the system, and at a reasonable cost.

1.1.c.ii Chip-scale Computer interconnects

Chip-scale packaging represents the highest density of circuitry possible. Bare, processed chips are thinned and stacked to create a small three dimension module. To date, this technique has been demonstrated and successfully commercialized for use in

memory chips. To expand this technique to processing circuitry which would dissipate more electrical power resulting in greater heating, methods of removing or preventing the creation of heat must be established. In either the memory or processing circuitry scenario there exists the same interconnect issues as faced in the stacked MCM architectures. Electrical interconnects tend to be limited to peripheral contacts and are therefore limited in density and number. Optical interconnects can play an important role in this type of extremely small computing module.

Chapter 5 explores an implementation of optical interconnects in stacked chip-scale modules. Issues such as system alignment and interconnect density are addressed as well as the technological advances required to demonstrate chip-scale computers.

1.2 Report Overview

This report presents subject matter from two U.S. Patent disclosures: Patent #5,652,811 "Semiconductor on Fiber Optic Substrate (SOFOS)" and "Optically Guiding Multichip Modules" (Patent Pending). Both the issued patent and the pending patent are authored by this report's authors. The ideas presented are the result of many years of building optical interconnects and fabricating electro-optic and micro-optic devices.

This report is divided into four sections with Chapter 1 giving a brief background in optical interconnects and the two packaging technologies that we are investigating, the MCM and stacked chip computers. Chapter 2 describes the optical guiding material that we propose to use in these systems. Chapters 3 and 4 describe in detail the implementation of optical interconnect scheme into such computer architectures.

2. Optically Guiding Substrates

2.1 Optically Guiding Substrates for Optical Interconnect Schemes

A novel method for integrating optical interconnects into MCM and stacked chip computer architectures centers around the use of fiber optic plates (FOPs) as part of the substrate material in the MCM or an actual chip. An FOP consists of a bundle of very

small diameter optical fibers that are fused together so that the fibers are all parallel to each other and perpendicular to the plate as shown in Figure 1.

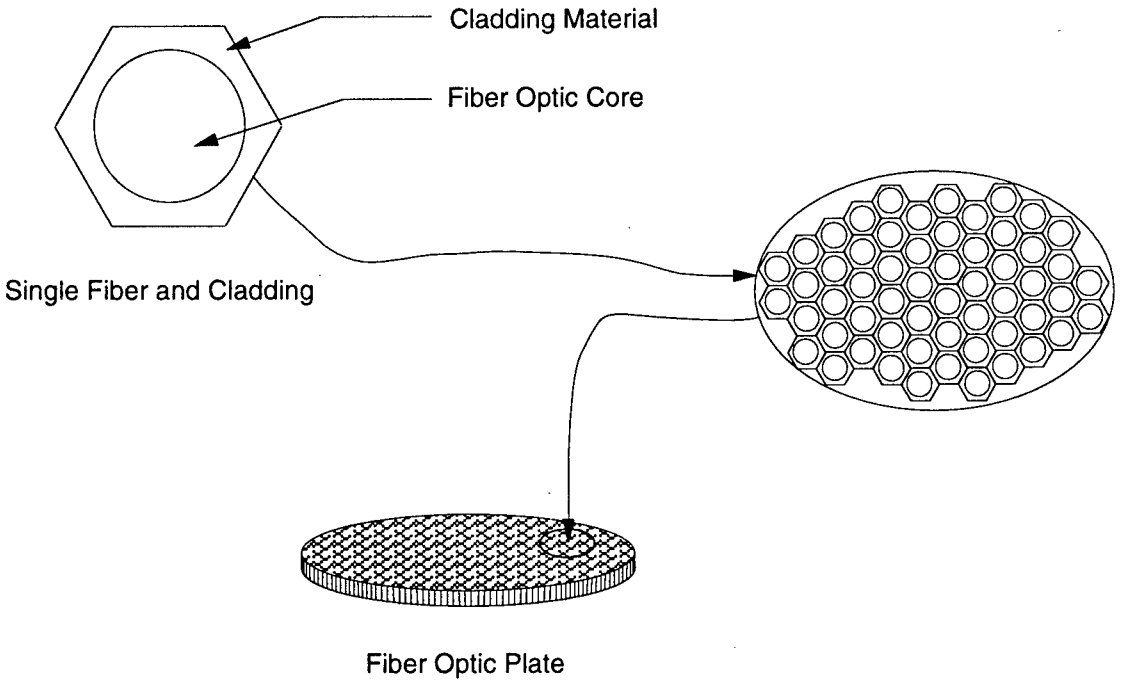

Figure 1. Drawing of a fiber optic plate with blown-up views.

FOP's are commercially available and can be manufactured in the sizes, thickness and center-to-center fiber spacing required for this application. A fiber spacing of 6 to 8 μm center-to-center is available and would be appropriate for this system. The spacing is fine enough that the fibers form an essentially continuous bundle of wave guides through the plate. The effect of this optically guiding material is to transfer a pattern of light from one side of the plate to the other with very little image spreading as is indicated in Figure 2 where a 3 mm thick FOP is placed over a light emitting diode (LED). A microscope was first focused on the LED itself (Figure 2.a) and then on the image of the LED as it was translated through the FOP (Figure 2.b). As can be seen, there is little image distortion or divergence of the optical pattern. The Lambertian output profile of LED's typically make them unsuitable for optical interconnects due to the difficulties associated with collecting the broadly divergent output.

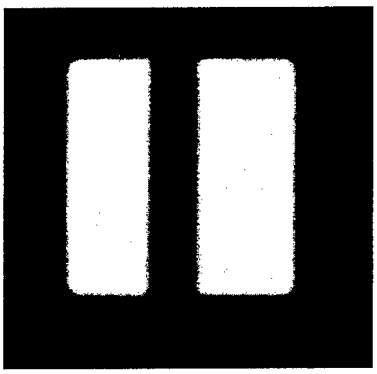

Figure 2.a Optical micrograph of a, 50 μm x 50 μm LED. The center stripe is an electrical contact.

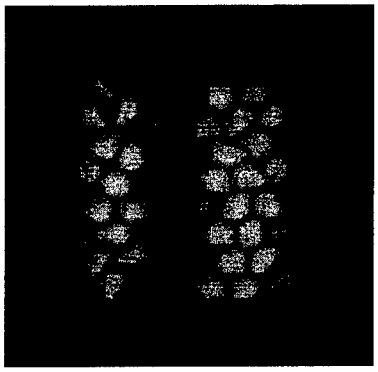

Figure 2.b Optical micrograph of the same LED covered with a 3 mm thick fiber optic plate.

Besides the obvious image translation ability of FOPs, there is another advantage of using this material in optical interconnect schemes. The "optical imaging system" (the FOP material) does not have to be aligned. In most optical interconnect schemes a lens (a diffractive, refractive or holographic optical element) is used to focus the light from an optical emitter to a detector, all three elements (emitter, lens, and detector) would have to be aligned correctly in three dimensional space. However, when the FOP material is used to guide the light from emitter to detector, the emitter and detector must still be aligned to each other but no alignment is required of the FOP. The FOP can be shifted or rotated in the X and Y axis with no change in the light transmission from emitter to detector.

The alignment of the emitter to the detector can be aided by using alignment marks placed on the FOP material allowing for see-through substrate-to-substrate alignment. Figure 3 is a micrograph of a fiber optic plate placed over an alignment mark. The 6 to 8 μm diameter fibers can be seen and the image of the alignment mark, though translated 1 mm, has little distortion. The fiber optic plate can be translated in the X and Y axis with no affect to the translation of the alignment mark image. It does not matter which of the micro-fibers the image passes through. These concepts will be explained further in the following two chapters.

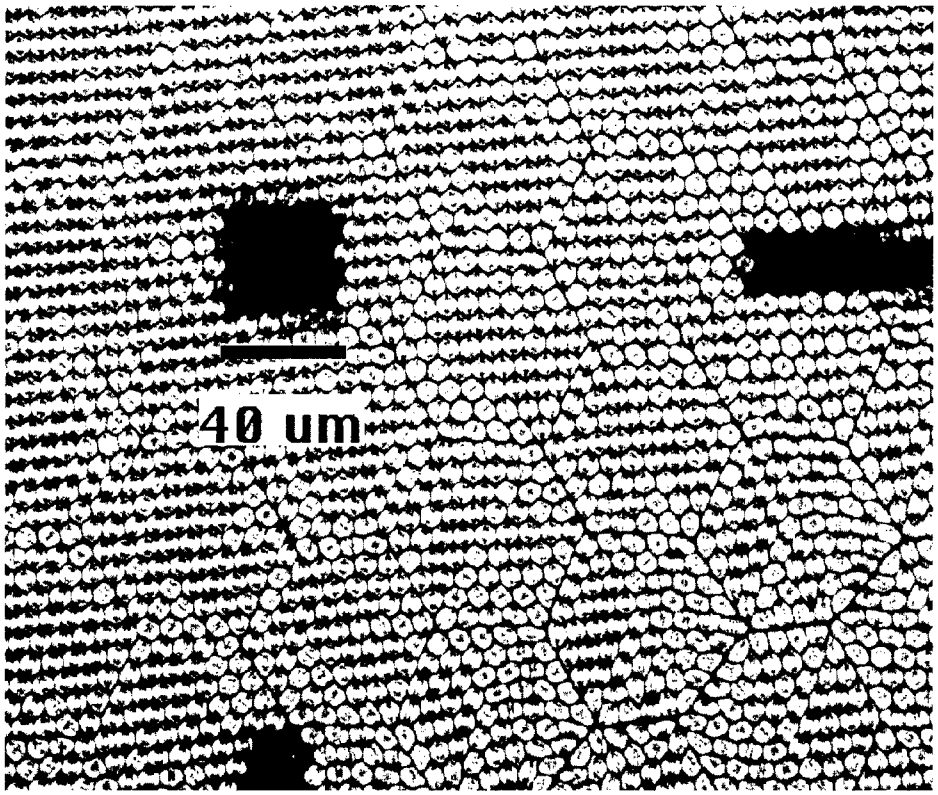

Figure 3. Micrograph of a backlit chrome mask (the square in upper left) viewed through a 1 mm thick fiber optic plate. The fiber cores are 6 μm in diameter.

2.2 Fiber Optic Plate Fabrication

The FOP fabrication process is shown in Figure 4. The plates are made by first making a preform similar to those used in the fabrication of fiber optic cables. The preform is made from two kinds of glass, a high index material for the central core and low index material for the outer cladding. Unlike in fiber optic cable preforms, the core in this case is a much larger percentage of the total preform diameter than the cladding. In order to establish an optically guiding path with such a thin cladding layer, the difference of index of refraction between core and cladding is greater than in fiber optic cables. In the final plate it is the core that transmits the image through the plate and it is therefore advantageous to limit the area taken up by the cladding material.

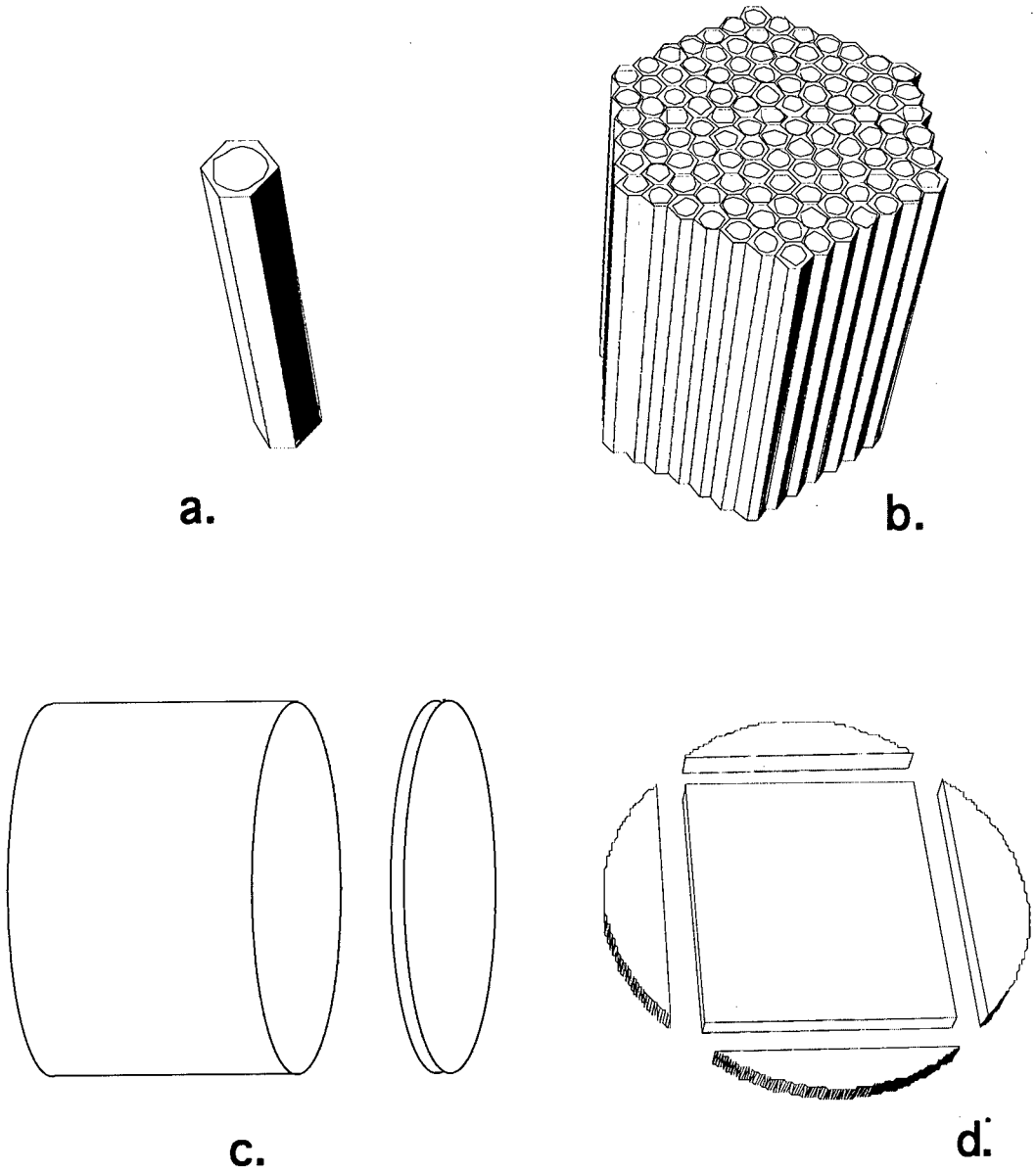

Figure 4. Fabrication steps of a fiber optic plate: a) fabricate a fiber preform and boule with large core to cladding ratio; b) fibers stacked, fused, heated and drawn; c) drawn fibers are cut, stacked, fused and drawn until desired core diameter is reached; e) final fiber optic bundle is sliced into plates.

The glass preform is heated to a plastic state to fuse the core and cladding layers forming a boule which is then heated and "drawn" to many times its original length. This long piece is then cooled and cut into short pieces. These pieces are then stacked to form a bundle, fused, and drawn again. This process is repeated until the final desired core diameter is reached as shown in Figures 4.b) - 4.c). The final step is to slice the resulting fiber bundle into plates of the desired thickness as shown in Figure 4.e). The

plates can be as thin as a typical silicon wafer used in chip processing (approximately 15 mils) to several inches thick.

2.3 Thermal Conductivity Issues of Fiber Optic Plate Materials

Currently FOPs are made from glass (SiO_2) because of the variety of refractive indexes and other characteristics such as its tendency to draw in an ideal manner. Because glass is a poor conductor of heat the FOP material has very low heat conductivity. This may represent a significant limiting factor to the use of this material in computer packaging where excess heat is detrimental to circuit performance and lifespan.

Materials used in electronic packaging have a range of functions and requirements. They are typically expected to conduct heat well, to be electronically insulating, and to have coefficients of expansion close to the semiconductor materials that they come in contact with or are bonded to. The FOP material is an ideal optical interconnect medium and it is electronically insulating but fails as a thermal conductor. Ideally, two materials (one for the core and one for the cladding) would be identified with acceptable thermal conductivities that could be formed into a FOP. These materials must be malleable enough to be drawn like glass, they must have coefficients of expansion close to each other over the range of temperatures required in processing, they should be fairly transparent in the visible wavelengths, and form at least a polycrystalline state when cooled so that the resulting plate is heat conducting. Without such a material the use of the FOP may be limited to packages with low power circuitry or only to areas of the package where optical interconnects and alignment marks are required. However, the required thickness of the plates is only 1 mm for MCM applications and 0.1mm for stacked chip applications which greatly relaxes the optical quality reqirements (i.e. transparency). In contrast fiber optic cables must carry optical signals over tens of kilometers so the material absorption at optical wavelengths must be minimized.

Material	Thermal Conductivity (W/m•K)	Melting Point (°C)	Linear Expansion Coefficient (x 10^{-6})	Index of Refraction
Air	0.026	—	—	1
Aluminum [Al]	200	660	23	-----
Alumina [Al_2O_3]	28-35	2050	8.0	-----
Aluminum Nitride [AlN]	165	2200	5.3	3.16
Beryllia [BeO]	300	2570	7	1.72
Copper [Cu]	395	1083	17	-----
Diamond [C]	2000	>3500	1.1	2.42
Fused Silica [SiO_2]	2.1	1100	0.54	1.46
Gallium Arsenide [GaAs]	50	1238	6.86	3.62
Gold [Au]	298	1063	—	-----
Sapphire [Al_2O_3]	42	2015	6.3	1.77
Silicon [Si]	150	1420	4.7 - 7.6	3.4
Silicon Carbide [SiC]	270	>2700	4.3 - 4.6	2.7
Zinc Oxide [ZnO]	67	1975	5.5	2.02

Table 1. Thermal and physical properties for popular electronic and packaging materials[11,12].

The physical properties of some materials used in computer packaging are listed above in Table 1. Most of these materials are listed for the sake of comparison. One can see that silicon is actually a very good conductor of heat. Ideally the heat conductivity of the FOP materials should be at least as good as silicon. There are two reasons for this. Taking a 1 cm^2 chip as an example, the chip can conduct heat through all of the 1 cm^2 area of its silicon substrate when mounted in a conventional manner. When mounted in a stacked chip array the heat must be removed via the edge of the chip. This area of this edge is 0.5 mm (the thickness) x 1 cm x 4 (the perimeter) which yields 0.2 cm^2, one fifth the area of a conventionally mounted chip.

In addition, the distance heat must travel between any circuit element and a heat sink is about 0.5 mm for a conventionally mounted chip. In a stacked chip array the heat must travel sideways an average distance of 2 or 3 mm. So the area the heat can be transferred across is 1/5 and the distance traveled is about 5 times which indicates that the temperature difference between the devices on the stacked chip module and the heat sink temperature could be 25 times higher than a conventionally mounted chip. Add to

that the fact that the FOP will probably have a thermal conductivity closer to sapphire than to silicon. These facts point out the difficulty of removing heat from any package of dense circuitry, not just an optically interconnected one. Fused silica has a thermal conductivity less than 2 percent of silicon. It is obvious that a big improvement is needed here.

Sapphire appears to be a good candidate for making a heat conducting fiber optic plate. Although its heat conductivity is less than that of silicon, sapphire could be a starting point for prototype systems. Preliminary tests indicate that sapphire forms a glassy state when it reaches its melting point. Upon cooling, the polycrystalline state appears to be transparent enough to be used in the fabrication of FOPs. Another material must be found that is compatible with sapphire in order to make up the fiber cladding. Zinc oxide may work here although tests need to be done to determine if it can be drawn as a glass. Another possibility is Ga_2O_3; gallium is just under aluminum in the periodic table so it promises to be a good match to Al_2O_3. Data on Ga_2O_3 is not plentiful so more research on its physical properties must be done.

3. Optically Guiding Substrates as Part of a Multichip Module

The designs presented in this section represent an attempt to introduce the capabilities of optical interconnects into the emerging multichip module designs. A major advantage of the proposed design over traditional optical interconnect schemes is the ease of alignment and the low cost of implementation. The fundamental objective is to develop a technology which will provide a high density, high speed, high reliability, and easily manufactured data buss for electronic circuits located on separate MCM's. These designs provide a practical means for accurately controlling the propagation of optical signals between MCM's and a practical means for aligning one module to another.

Typical MCM substrates are made of ceramics, fiberglass and resin, silicon, or plastics. The driving factors behind the type of material used have been cost, electrical performance, thermal dissipation, and mechanical support. We have included an additional performance criteria, the optical characteristics of the substrate. For optical signals to travel from electronics on the top of one MCM to the circuits on the top of another, the MCM must be optically transparent. To accommodate a large number of

optical channels in a small area with good channel isolation, the signals must be either imaged (focused) or guided between the emitters on one MCM to the detectors on the next. In our scheme the MCM performs the functions of providing a platform for dissimilar chip sets (i.e. silicon processors and gallium arsenide optical emitters) as well as a means of controlling the propagation of optical signals between different MCM's. The optically guiding FOP material is incorporated into the MCM in areas required for optical data channels and for visualizing alignment marks through the module.

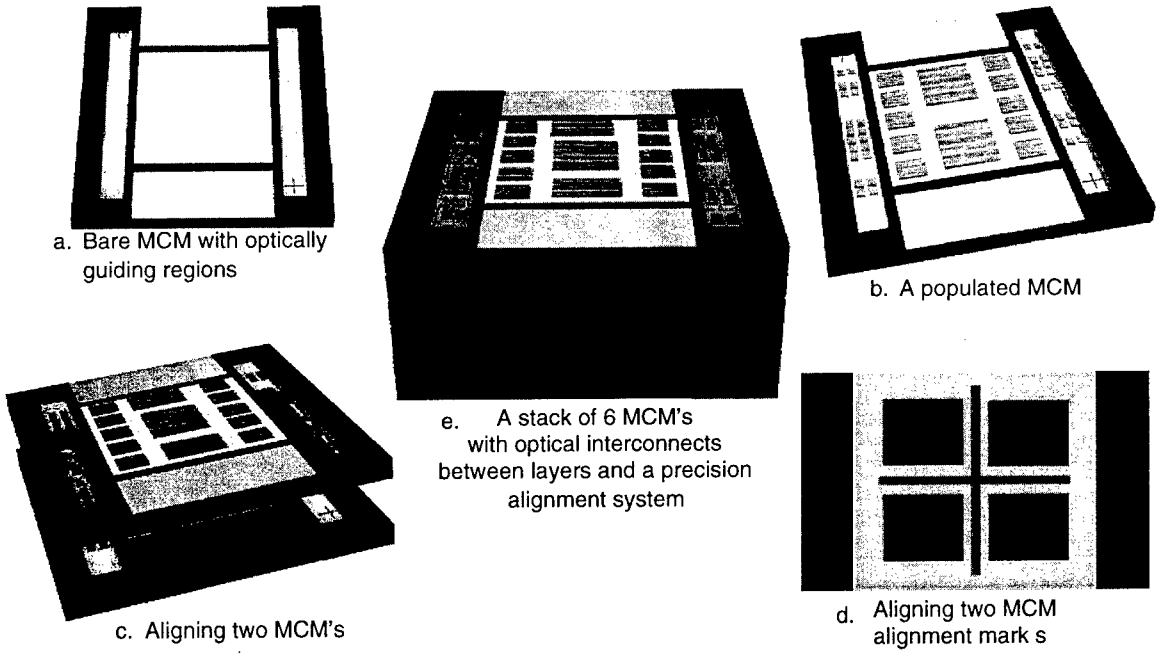

Figure 5. A conceptual diagram of a) a single multichip module with areas suitable for optical interconnects, b) an MCM populated with IC's, c) the process of aligning two MCM's, d) a method of using complimentary alignment marks on each MCM to align one to another, and e. a stack of 6 such MCM's.

Figure 5 depicts a computer comprised of a stack of MCM's with a large number of point-to-point optical data channels providing communications between MCM's. The steps of constructing the computer from a bare MCM in Figure 5.a) to the population of the module with integrated circuits in Figure 5.b) and the aligning and stacking of modules in Figures 5.c) to 5.d). Figure 5.d) is a top-down view of two overlaid MCM's where the alignment mark of the lower MCM (a cross) is seen through the complementary alignment structure (four squares) placed on the FOP region of the upper MCM.

A more detailed picture of the components of a single MCM is shown in Figure 6. Here the various functional regions are highlighted. The center section of the MCM is a standard ceramic or other material MCM sub-unit potted in a thermally conductive epoxy. The epoxy is shown here in black. The two strips to the right and left of the center MCM sub-unit are pieces of FOP material embedded in the epoxy in such a manner that it extends through the epoxy. The electro-optic devices (emitter and detector arrays) are mounted on the FOP material. The embedded pieces above and below the MCM sub-unit are pieces of high thermal conductivity material.

An on-MCM electronic interconnect scheme such as the General Electric High Density Interconnect[13] can be used to connect the processing circuitry found in the middle of the MCM with the electro-optic optical data buss devices. These interconnects would be photolithographically defined for high density. Where the FOP material is placed is largely dependent on the material used for the MCM supporting the processing circuitry and whether a piece of FOP can be embedded into it. Ideally the interconnects would be located throughout the MCM close to the originating and receiving circuitry.

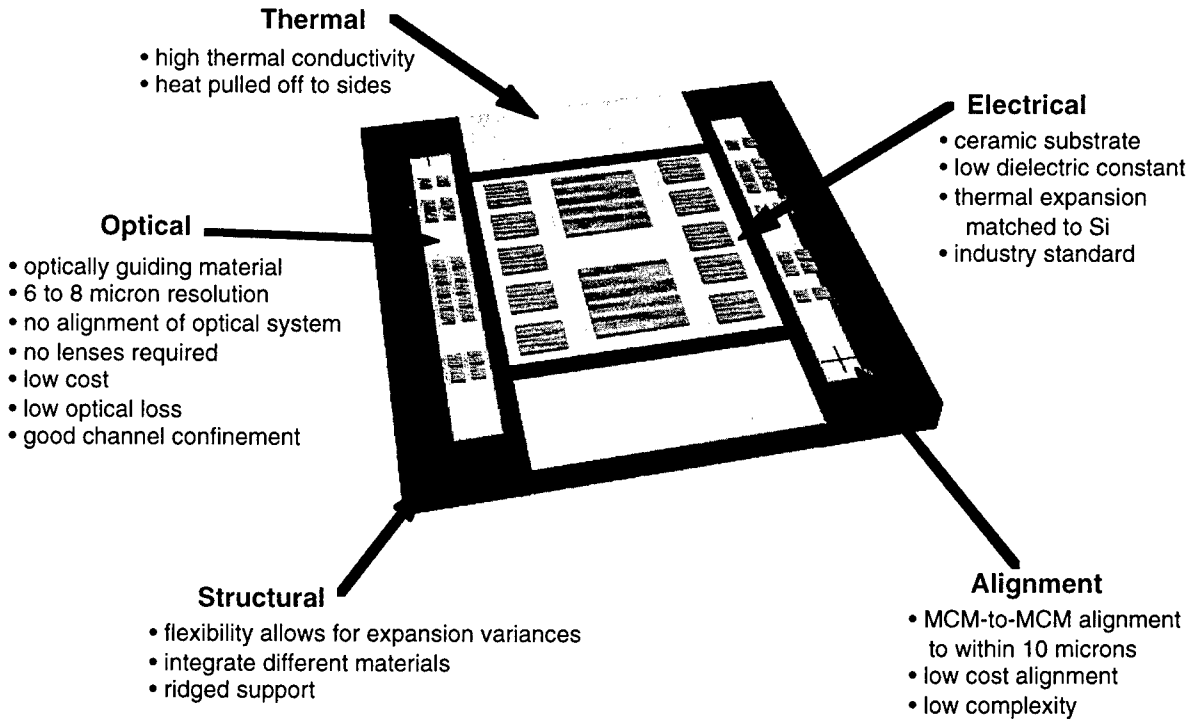

Figure 6. A conceptual drawing of a multichip module with areas optimized for electrical, thermal, mechanical, and optical performance.

3.1 Implementation

A Fiber Optic Plate (FOP) is used as a multichip module (MCM) substrate or, as is more likely the case, as a part of a multichip module substrate in order to guide optical signals from circuitry on the top of one module to circuitry on the top of another module in a stack of FOP MCM's.

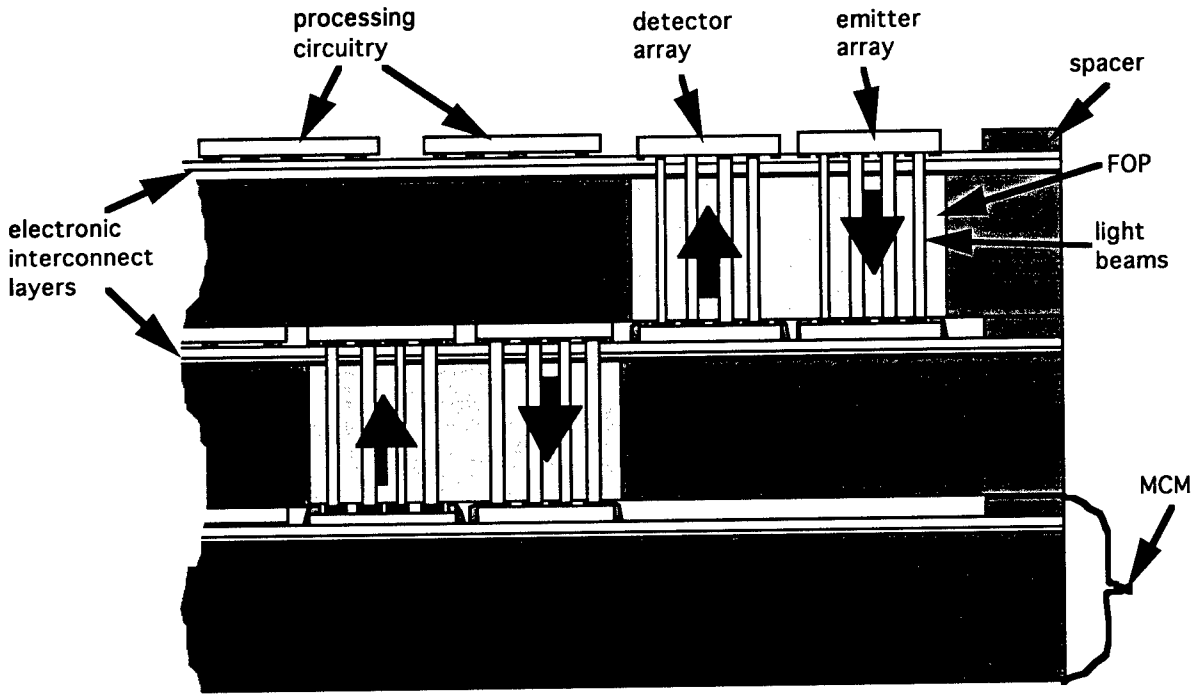

Figure 7. A cross section of a stack of multichip modules with optically guiding material embedded into the MCM substrate in areas required for optical interconnects.

A cross section of a stack of FOP MCM's is represented in Figure 7. The embedded FOP material extends through the MCM substrate providing an optical path between emitter and detector arrays on different layers. Light incident on one surface of a FOP MCM will be confined to the fiber cores which comprise the FOP and will be translated to the other side of the MCM without the divergence normally associated with light traveling through air or a uniform transparent medium. The optical signals are represented by the lighter colored areas with the direction of travel of the light beams indicated by the large black arrows. The optical emitters and the optical detectors will be fabricated with the same device spacing and configuration to insure the proper alignment

of each emitter to each detector. The light from a single emitter will be incident on a single detector creating an optical data path.

A "chip-last" design is depicted here where the in-plane electronic interconnect layer is established first before the chips are in place. A "chip first" approach such as the General Electric High Density Interconnect (HDI) could also be implemented. A means of allowing light through the electronic interconnect layer must be devised either by using optically transparent materials (such as is the case in the HDI process) or holes must be fabricated in the medium. A thin spacer may be employed between MCM's to prevent pressure from being applied directly to the chips. Power and ground connections can be run along the perimeter of the MCM stack and connected to external power supplies via pressure or solder contacts.

As is readily apparent from Figure 7, the ability to transmit optical signals both up and down requires emitter arrays which emit up and arrays which emit down. Likewise there must be detector arrays which receive light from above and others that receive light from below. Such devices exist, though their use is complicated by the need to standardize the method of electronically bonding these different devices to the MCM in order to ease system construction. Therefore, some emitters will have to emit from the side of the chip with the bonding pads while others must emit through the chip substrate. Likewise half of the detectors will detect the light from the side of the chip with the bonding pads and half will detect through the chip substrate. Emitting through a substrate adds some beam divergence (the substrate can be fabricated with a different absorption profile than the emission region of the device) while detecting through a thick substrate is not possible due to the absorptive nature of the detector material. Chip thinning and wafer bonding to thin FOP substrates will be explored as methods of fabricating emitter and detector arrays which emit and detect from both front and back sides.

3.2 Advantages

The optical guiding nature of the material used allow for a much higher number of optical interconnects in a smaller space and at higher bit rates than is possible with traditional board-to-board electronic interconnect methods. The density of optical channels is limited by how well the individual emitter and detector pairs can be aligned to

each other. With perfect alignment the resolution of the FOP material would support 50μm center-to-center spacing of devices but the real-world alignment constraints require a larger device spacing. We believe that 125μm center-to-center spacing of devices will be within the capabilities of standard alignment systems. Each optical channel can operate at bit rates over 1 GHz. Micro-laser arrays containing 16, 32, or 64 devices can be fabricated along with corresponding photodetector arrays.

The ability of the FOP to collect the light from a source and to guide the optical image to an optical detector with little distortion leads to very little loss of the optical signal and extremely low noise from adjacent optical channels. The amount of optical power that must be generated by the optical source for each bit of data can therefore be reduced compared to more lossy interconnect schemes such as diffractive optic and hologram based systems.

The FOP MCM design presented here allow for much lower alignment tolerances and device performance in comparison to other optical interconnect schemes found in the technical literature. This scheme is not dependent on high cost optical devices or alignment requirements. This scheme can accommodate either low cost light emitting diodes (LEDs) or higher performance vertical cavity surface emitting lasers (VCSEL's). The MCM stack can be disassembled and reworked easily because of the lack of hard wired electrical interconnects. The following sections will discuss these advantages in further detail.

3.2.a System Alignment

3.2.a.i Importance of Low Alignment Tolerance

A critical factor in the successful implementation of any optical interconnect scheme is the ease of aligning the components. Unlike optical interconnect schemes which use lenses, diffractive optics or holograms to redirect or refocus divergent light beams, the FOP does not have to be aligned to the optical source or the optical detector. The light guiding function is part of the support structure of the computer. It is part of the computer board which holds the integrated circuit chips. The fibers which make up the FOP have a uniform distribution which means that the FOP simply needs to be placed

between the optical emitter and optical detector. It does not matter which fibers carry which optical signals.

A second factor which greatly enhances the alignment of one FOP MCM to another is the capability to see through the FOP's so that one plate can be aligned to alignment marks on the plate below it. This capability can be enhanced by the use of a light source placed below the two plates or by optical emitters on the first plate. Alignment to within the core size (approximately 6 to 8 μm in diameter) of the individual fibers which comprise the FOP is possible.

3.2.a.ii Alignment Method

One of the major issues that this optical interconnect scheme addresses is the ease of alignment of one MCM to another. It is critical that the large number of optical signals generated on one FOP MCM reach the corresponding photodetectors on the adjacent MCM with little crossover or crosstalk between channels. The method of aligning the system must be within the capabilities of the system manufacturers without undue cost for precision alignment tools or expertise.

The alignment of the proposed FOP MCM is a two-staged process. First, the integrated circuit and optical transmitter and detector chips must be aligned to the individual MCM. The chips are aligned to a fixed reference point on the MCM such as the alignment mark shown in Figures 5 and 8.

The second stage of the alignment process is the alignment of one MCM to another. Two alignment schemes are depicted in Figure 8. and can be used independently or in conjunction with each other. In Figures 8.a and 8.b a circular aperture is placed on each FOP MCM. An external light source, shown as a light emitting diode (LED), is placed beneath the aperture and the MCM is moved until a maximum signal is transmitted through the aperture. A second MCM is placed over the first and the alignment process is repeated. This process is repeated for as many FOP MCM's as required in a stack. This process may be automated by the use of a segmented detector (i.e. a quad cell detector) placed above the aperture which indicates the direction of misalignment.

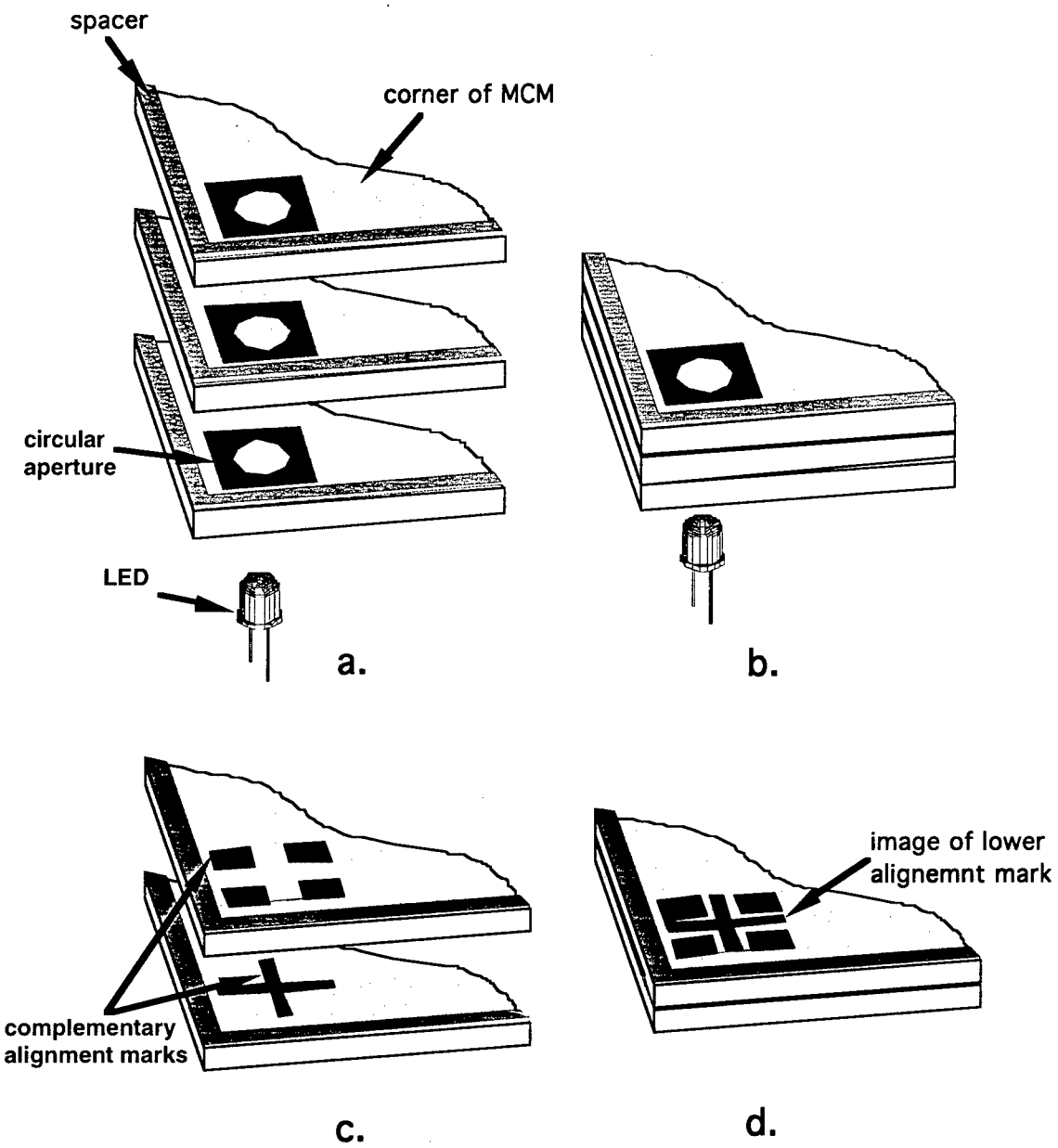

Figure 8. Two alignment techniques for aligning two or more multichip modules with optically guiding substrates to allow for see-through alignment with a high degree of resolution. a. & b. Alignment with an external light source and circular apertures. c. & d. Alignment with complementary alignment marks.

The second alignment scheme depicted in Figure 8.c and 8.d uses complimentary alignment patterns on adjacent FOP MCM's. In this case a cross is patterned on one FOP MCM and a pattern of four squares is placed on an adjacent FOP MCM. The image of the cross can be viewed through the upper FOP MCM and accurately aligned to the four square patterns.

The module-to-module alignment capability is limited only by the core size of the fibers of the module which limit the resolution of the alignment mark image. The typical core size of 6 to 10 μm provides a much better alignment capability than current multichip module alignment capabilities by other methods and is well within the alignment requirements of the proposed optical interconnect scheme.

3.2.b Rework Capability

The FOP MCM design has significant reliability and rework advantages over traditional packaging methods. Electronic connections require a physical connection formed by either a pressure contact or a soldered joint. These are potential failure points due to repetitive insertion wear of pressure points or thermal expansion induced solder cracking. As the number of interconnects increases the potential for failure increases. Pressure contacts can be limited in interconnect numbers by the force required to insert a module while solder joints or other "hardwired" interconnects must be stripped and reapplied if rework is required. The optical interconnects detailed here are established by the light traveling through a light guiding substrate; there are no physical metal contacts to wear down. Rework is simply a matter of separating the modules and realigning the system afterwards.

3.2.c Low Cost & Complexity

A fundamental reason for the absence of commercially available optical interconnect technologies is the cost of implementation. Interconnect designs have been demonstrated in laboratories with little input or notice by computer packaging engineers. To make the leap to a commercial product the following capabilities must be proven: that electro-optical devices are cheap, stable, and offer a performance advantage over electronic devices and that the proposed architectures are manufacturable. The main driving factor in manufacturability is cost and one of the most expensive tasks is system alignment.

In many optical interconnect schemes the complexity of specialized micro-optics and the precision alignment required for initial assembly and long term operation make

these systems cost prohibitive. Many systems are dependent on devices which are hard to manufacture (i.e. diffractive or holographic optics), are environmentally unstable (i.e. VCSEL's), or require extremely tight operating tolerances (i.e. SEED's) which drive system costs out of the reach of the commercial market. Alignment of optical emitters, one or more optical focusing devices, and detectors through free space is extremely undesirable from a large scale manufacturing perspective. The FOP MCM design overcomes these limitations by decreasing the tolerances on alignment and device performance.

3.3 Design Limitations

There are three main limitations to the FOP MCM concept. First, it is unclear whether there is a suitable method for integrating the FOP material with standard electronic packaging materials such as alumina substrates. Second is the problem of inserting a material with poor thermal conductivity into a dense electronic packaging environment. The third problem is that the proposed concept represents a radical shift from standard packaging techniques. The packaging community is reticent about changing from established methods of doing business.

Ideally, a single material would be able to meet all the performance requirements of an MCM substrate. It would have a high thermal conductivity, be electronically isolating, mechanically stable, optically transparent and suitable for configuring into an FOP, and be very inexpensive. Unfortunately, no known material meets all of these requirements; good thermal conductors tend to conduct electricity and be optically opaque. Two notable exceptions to this trend are diamond and sapphire which meet all requirements except for low cost (in the case of diamond) and the ability to form into FOP material.

In applications which do not require thermally conductive substrates, an MCM made completely of FOP can be used. However, most applications will require a high heat transfer capability, especially in a stacked MCM configuration where there is a high density of power dissipating circuits. For these applications a hybrid MCM substrate is proposed. FOP material can be inserted, or potted, in a material with a higher thermal conductivity. The FOP must extend completely through the substrate allowing optical signals to pass through the MCM. In areas requiring additional thermal conductivity and

good electrical characteristics another material can be inserted into the substrate material such as Al2O3, AlN, or Si. A copper plate can also be inserted to draw heat to the edge of the module. The resulting hybrid MCM must be planar, mechanically stable, and withstand the different expansion coefficients of the potted subunits.

4. Optically Guiding Substrates in Chip Scale Packaging

4.1 Background

The performance of high speed computers today is limited by the connections between integrated circuits within the computer[14]. The printed circuit traces used as chip-to-chip interconnects cause problems with signal latency, signal speed, crosstalk, and excessive power dissipation by the integrated circuits themselves. One way to reduce the severity of these problems is to make the traces as short as possible by bringing the microchips closer together. This can be done by reducing chip package sizes or doing away with chip packaging and mounting bare chips directly on the circuit board itself as is done in MCM's.

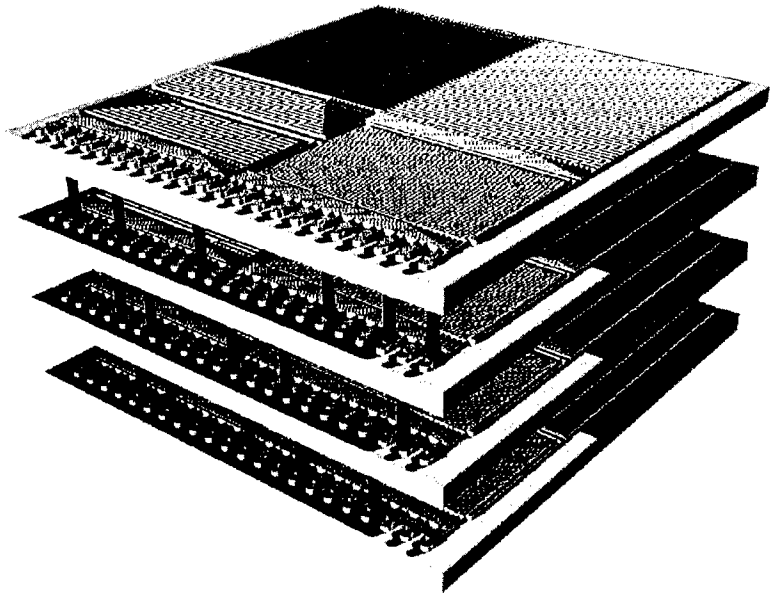

Figure 9. An exploded view of a chip stack with optical interconnects providing chip-to-chip data transfer.

Ultimately, the shortest traces possible are established by stacking the chips directly on top of one another as depicted in Figure 9. Currently some memory chips stacks are being made this way but problems with traces exists since the traces are run to the edge of the chip, up or down to the edge of one of the adjacent chips, then back into the interior of that chip. This produces traces longer than the package dimensions and limits the number of connections from one layer to the next since the traces are still being run through the same folded plane as in the circuit board. Ideally, one would like to run wire connections directly through the substrate of one chip to an adjacent chip. Currently there is no technology that allows this.

Instead of electricity, we can use light beams to transmit high speed data from one circuit layer to another. This would allow the direct connection of one layer to the next, shortening the path of the connection by as much as an order of magnitude and increasing inter-chip speed by at least the same. With signals carried on light beams instead of wires the risk of relying on thousands of solder joints is eliminated. In addition, the expense of providing "known good die" is relieved in two ways. First, the manufacturer could qualify the die by providing the proper signals via light beams instead of using wafer probe technology with all its attendant difficulties. Or the manufacturer could elect to stack untested die then use diagnostic programs to identify any bad die. Since the die are not hard wired the faulty chip could easily be removed and replaced.

In order to implement optical interconnects in a stacked chip module a method of guiding the light from one layer to another must be used in order to overcome spreading due to diffraction. Alternatively two layers could be thinned and placed so close together that no appreciable spreading of the light would occur even without an optical imaging system. Likewise, metal contacts may be established between the thinned chips. There are several problems with either of these approaches. The removal of the substrates represents the removal of a significant thermal path in both of these cases. Also, in the case of the metal to metal contacts once the electrical contacts have been made the stack cannot be taken apart for repair and then reassembled. That means that known good die must be used in the stack which drives up cost and may be impractical with high speed chips.

4.2 Implementation

We propose the use of fiber optic plates (FOPs) as the bulk chip substrate in a stacked chip computer. The material is optically transparent, and optically guiding with a resolution of 6 to 8 μm. In this approach the FOP is introduced at the wafer level before the integrated circuit is fabricated. Figure 10 shows the basic construction of such a wafer. Two methods of constructing such a wafer are described below.

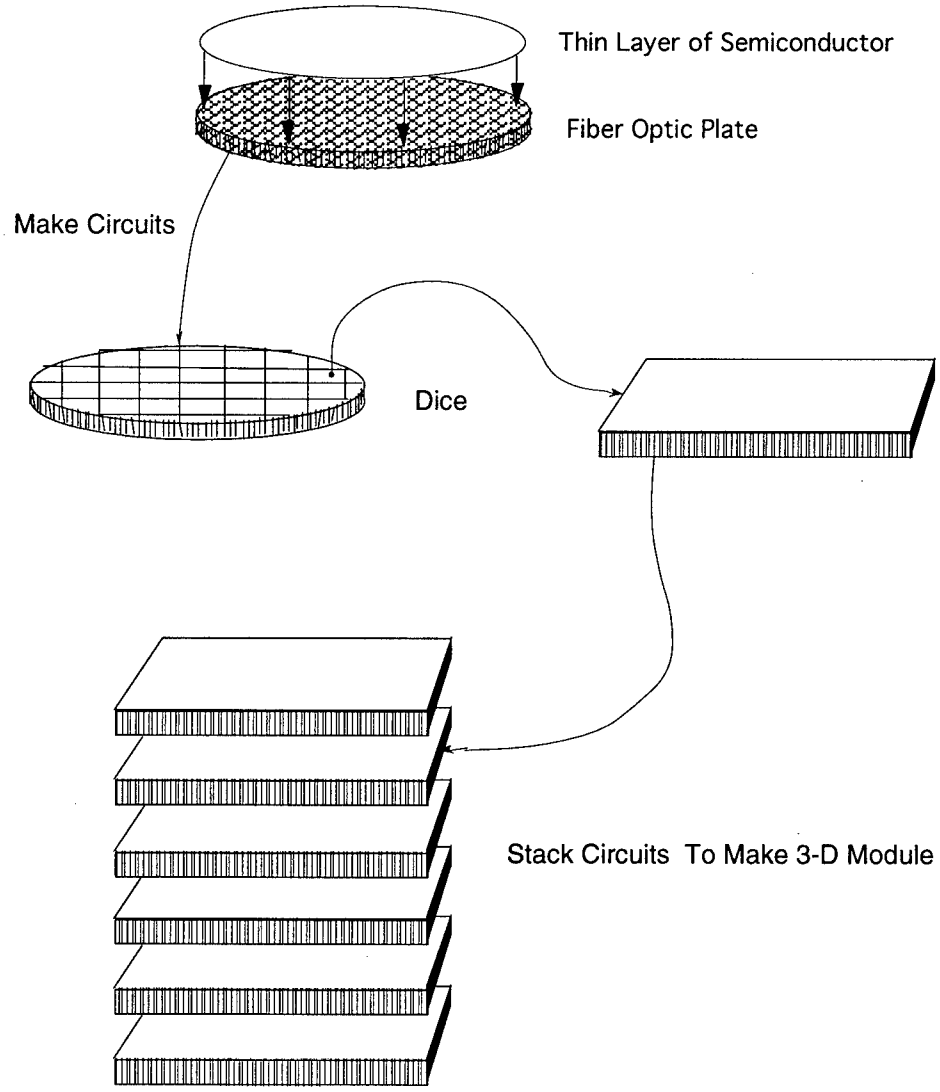

Figure 10. Construction of a semiconductor on fiber optic plate wafer and illustration of circuit stacking.

4.2.a Semiconductor-to-FOP Wafer Bonding

In the first method the fiber optic plate is pressed against a standard semiconductor wafer and since both surfaces are polished to a high degree of flatness van der Waals force hold the two plates together. Heating completes the molecular bond between the wafers. The silicon wafer can then be ground to a thickness of ten or so microns. The fiber optic plate is now the substrate for the electronic semiconductor layer.

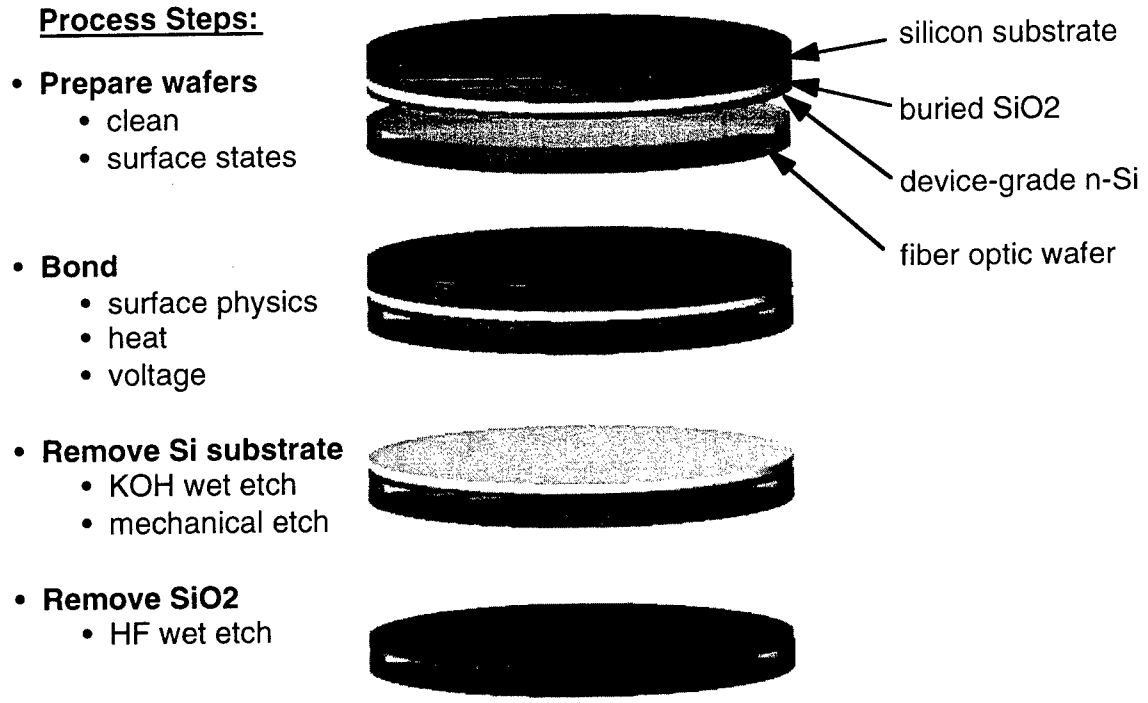

Figure 11. A wafer bonding process. In this example a silicon wafer is bonded to a glass plate and the bulk silicon substrate is removed leaving a thin device grade semiconductor layer bonded to a glass wafer.

An alternative method of bonding a very thin layer of semiconductor to a fiber optic plate is outlined in Figure 11. First, a layer of selectively etchable material is grown on a standard semiconductor wafer. Next, a layer that will be used to make electronic devices (integrated circuits) is epitaxially grown on top of the first layer to any desired thickness. A protective layer, for instance an oxide layer, can be deposited on this. The wafer is then bonded to the fiber optic plate as in the first technique. The semiconductor side is ground down close to the etchable layer and a selective etch is performed leaving

the electronic layer on top. This can then be processed to make integrated circuits as any other wafer would. A similar technique is used to fabricate of silicon-on-insulator wafers.

In both of these techniques the thinness of the layers is important in that a light detector or emitter can be constructed to be active on both the top and bottom so that signals can be sent/received from the top, as is normally done, or from the bottom, through the fiber optic substrate. It is this feature that makes it possible to stack the circuits (see Figure 12). Alternatively, if electronic interconnects were used, vias passing through the substrate would have to be constructed or wires would have to be brought out to the edge and back in to make the connections.

4.2.b Assembling a Stacked Chip Computer

An optical buss scheme for a stacked chip module is shown in Figure 12. Each layer has a group of emitters and detectors allowing that layer to send/receive data from/to adjacent layers. Communication directly between any two layers is also possible by simply etching away holes in the intervening layers. The direction the light is traveling is indicated by the arrows in the light columns of the fiber optic layers. When one layer initiates a signal the light is detected by the detectors in both directions on adjacent layers. This process is repeated up and down the stack until all the emitters are on. After a delay the emitters and the detectors are reset making them ready for the next signal.

Figure 13 illustrates means for connecting a stacked-chip module to a printed circuit board. Wire connections are brought out from an interface chip located at the bottom of the stack so it can then be easily connected to the printed circuit's connections to devices outside the chip. The whole stack could be flip chip mounted using bump bonds as shown. These connections would not have to be as high speed as the optical connections internal to the chip stack since peripheral devices do not require the speed that is required in the computer proper. Traces for power and ground are brought out to the edges of the chip modules. These traces are then connected together to a wire or printed circuit trace where the multichip module can be fed power and ground return. A similar technique is commonly used in memory stacks currently in production.

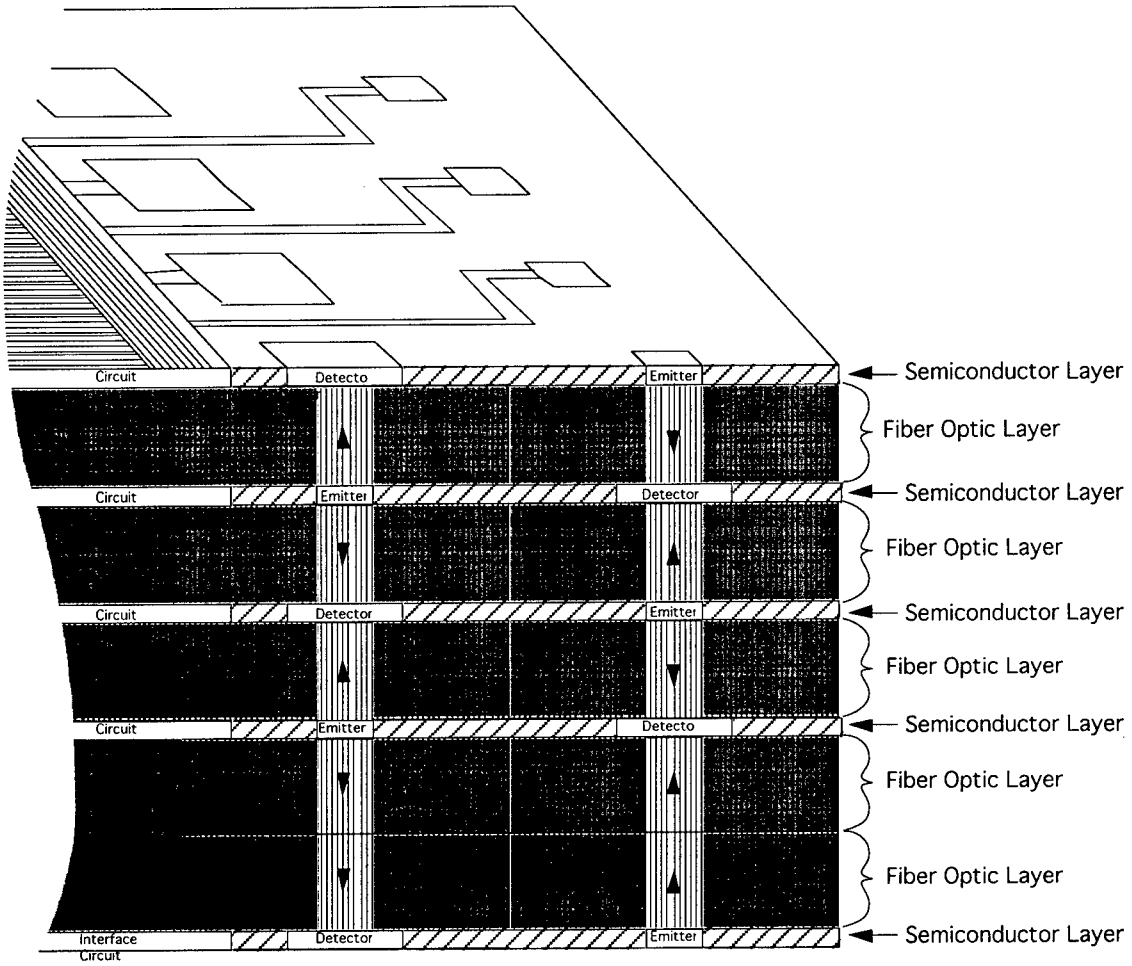

Figure 12. Stacked chip module with optical buss.

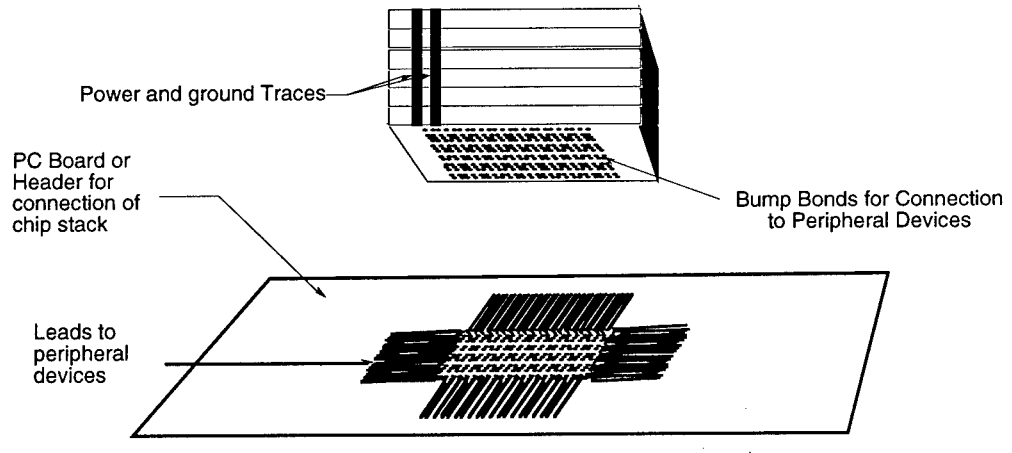

Figure 13. Interfacing the stacked chip module to a PC board.

4.3 Required Technologies

The use of this approach requires that the following basic technologies be in place: the integration of electro-optic and processing circuitry, substrates that allow transmission of light, means of guiding or focusing the optical beams to overcome the effects of diffraction (beam spreading), methodology to get heat out of the chip stack or to reduce heat production, and the ability to easily align all the layers. We will address these issues in the paragraphs below.

4.3.a Integration of Electro-Optic and Processing Devices

It is important to understand the VLSI circuit technology that we want to interconnect using optics. The only existing commercially viable VLSI technology is silicon based. The techniques necessary to fabricate VLSI circuitry exist because of decades of material and processing research focused on silicon. There is no other material technology that is mature enough to support the large VLSI circuit market.

A monolithic approach to integrating optical interconnects with traditional silicon circuitry requires that silicon chips emit light. Since silicon is an indirect bandgap material it does not naturally emit any appreciable amount of light. Attempts to get silicon to emit light, such as erbium doping or through the use of porous silicon have yielded some results but problems with these approaches persist. Other methods such as light emitting polymers that could be spun onto a silicon wafer show some promise but for high speed interconnects a relatively high light output is required. At least 0.1 mW per interconnect would be needed to meet system needs. Light emitting polymers currently have a few percent efficiency which would mean driving a small (less than 100 μm square) emitter with 1-10 mW of power. All reports to date indicate that these emitters burn out before reaching this power per area output; polymers are organic and are much more susceptible to heat damage than crystalline devices.

Another approach is to make devices using a direct bandgap material like AlGaAs and transferring the devices to an already fabricated silicon chip. Epitaxial liftoff is such a technique although problems with device failure after transfer has been a problem. Because we need hundreds of light emitters to be successfully transferred this is not a good technique for our application.

An approach that is related to the epitaxial liftoff technique is Wafer Bonding. In this technique a GaAs wafer is prepared by first growing an etchable epitaxial layer. On top of this VCSEL (or LED) layers are grown (Figure 14). This wafer is then pressed against a FOP and van der Waal bonds cause the two wafers to stick together. The resulting sandwich is heated in vacuum to complete the bonding. The entire structure is then put in a selective etch solution and the etchable layer is removed allowing the GaAs substrate to be detached. The same procedure is now followed with a silicon layer that is mounted on top of the GaAs layer (Figure 15). Standard silicon circuits can now be fabricated in the thin silicon layer. Once that is accomplished the silicon can be etched down to the GaAs layer and VCSELs or LEDs can be defined. Traces can easily be run from the circuits to the light emitters. Detectors can also be made in the GaAs layer and connected in the same way. Emitter driving circuitry and detector circuitry can be constructed in either the silicon layer or the GaAs layer.

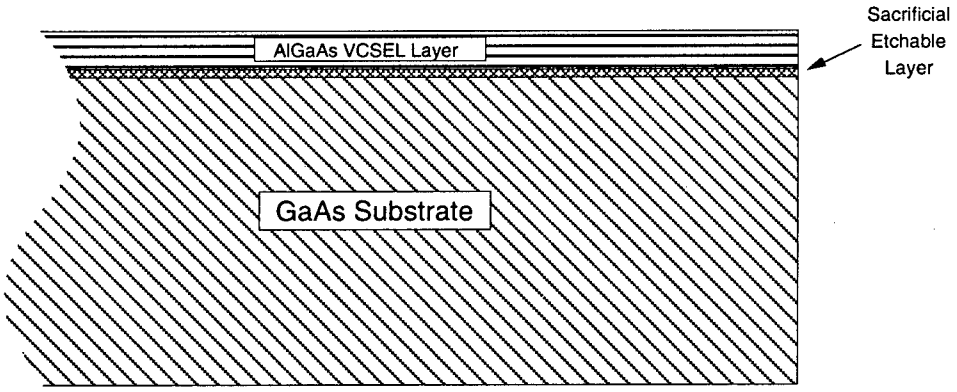

Figure 14. GaAs wafer with transferable VCSEL layer.

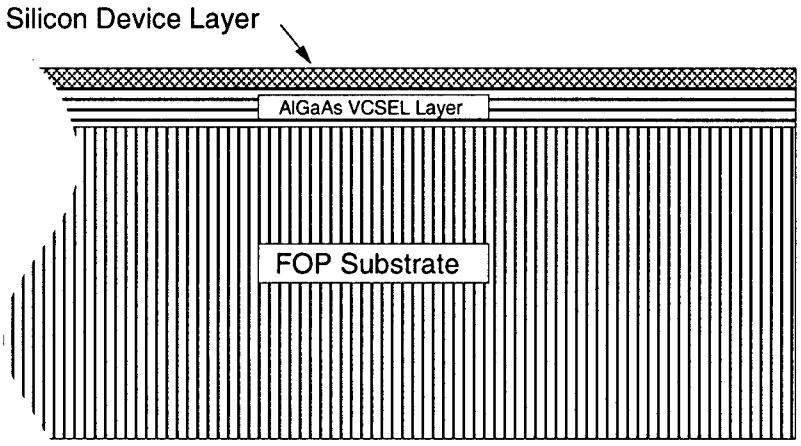

Figure 15. Profile of silicon on GaAs on FOP wafer.

It should be noted that although many of these techniques have been used separately using them together this way has not been done. The silicon on GaAs layering, in particular, has not been tried. Part of future efforts on this project would be to study the feasibility of building such wafers and then proceed with attempts to fabricate them. In addition VCSEL yields will need a significant improvement before we can use them for an application where hundreds of VCSELs must work without one failure. Initially LEDs may offer the reliability and cost needed.

4.3.b Thermal Management

As discussed at length in sections 2.3 and 3.3, thermal management is a major concern in dense circuit packages. Extraction of heat is an even greater challenge in stacked chip computers than in MCM designs because there is little thermal mass to transport heat away from the circuirts. Adequate cooling of a stacked chip computer will probably include a combination of the following tecnologies: low voltage level logic circuits, high efficiency optical emitters, an agressive cooling of the sides of the chip stack, and, as previously discussed, a higher thermally conductive FOP material.

5. Conclusion

The limitations of electronic interconnects are well established, particularly board-to-board interconnects where current interconnect methods are limited in number, reliability, and data rate. These limitations will become more apparent as computers become smaller as in stacked MCM and stacked chip systems. Ideally, these interconnects would be transparent to the processing circuitry with thousands of interconnects connecting computer boards at rates at least as fast as the processor(s) data rates.

Optical interconnects have long promised to offer such a level of interconnection. Unfortunately, the lack of mature device technologies and suitable system architectures have prevented optical interconnects from gaining a foothold into computer systems. Many of the optical and electro-optical devices are costly to fabricate and complex to implement. The optical interconnect schemes that use these devices often require such a high degree of alignment accuracy that they can only be assembled in research laboratories. The costs associated with these devices and the proposed architectures outweigh any performance enhancements these optical interconnects have to offer.

We have proposed a fairly simple optical interconnect concept with realistic alignment tolerances and without complex optical devices. By integrating an optically guiding material directly into the structure of the computer we remove the need to align the optical imaging system. The optically guiding material also aids in the alignment of the circuit layers. The guiding nature of the material provides an almost ideal imaging system able to transport high density optical beams between arrays of emitters and detectors on separate circuit layers.

There are a number of technical issues which must be resolved before the concepts presented here can be fully implemented. Specifically, methods of integrating the FOP material into an MCM must be devised which are manufacturable and do not detract from other elements of system performances. Also, a more thermally conductive FOP would greatly enhance the utility of this material. Packaging technologies such as flipchip bonding and wafer bonding must mature for the assembly of both the MCM and stacked chip architectures. The optically interconnected stacked chip computer requires either a method of making silicon emit light or a method of intimately integrating an electro-optical material with silicon. And finally, methods of aggressively cooling dense circuit

structures and methods of reducing the production of heat in electronic and electro-optic devices must be developed.

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☆U.S. GOVERNMENT PRINTING OFFICE: 1998-610-130-61229